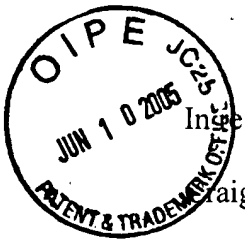
DFW

Docket No.: 043876-0145 **PATENT**



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig HANSEN, et al.	:	Confirmation Number: CNF NO. 3618
Application No.: 10/646,787	:	Group Art Unit: 2183
Filed: August 25, 2003	:	Examiner: Henry TSAI

For: PROGRAMMABLE PROCESSOR WITH GROUP FLOATING-POINT OPERATIONS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Applicants are submitting to the Office a single paper copy of each of the documents listed on the attached form PTO-1449 in connection with a corresponding Supplemental Information Disclosure Statement filing for U.S. Patent Application No. 10/418,113. Applicants are separately filing a Petition requesting waiver of Rules 1.4(b) and 98(a)(2), which requires copies of the documents listed on the attached form PTO-1449 to be provided herewith. In view of the Office's practice of scanning documents into the Image File Wrapper, it is believed that providing a single set of paper copies will enable the Office to process the papers efficiently and expedite the Examiner's consideration of the same. Furthermore, the attached form PTO-1449 includes citations

to some materials for which it is difficult to obtain additional copies. In view of the Petition and in the interests of efficiency, Applicants' respectfully request that a copy of each of the cited documents be made of record in the present application.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

In accordance with 37 CFR 1.17(p), please charge the fee of $180.00 to Deposit Account No. 500417.

Applicants bring to the Examiner's attention the following pending applications of Craig C. Hansen et al., which may include subject matter related to the present application:

Application Number	Title
10/418,113	Multiplier Array Processing System With Enhanced Utilization At Lower Precision
10/436,340	System With Wide Operand Architecture, And Method
10/616,303	Programmable Processor And Method With Wide Operations
10/705,946	Programmable Processor And Method For Partitioned Group Shift
10/712,430	System And Software For Catenated Group Shift Instruction
10/716,561	Programmable Processor And Method For Matched Aligned And Unaligned Storage Instructions
10/716,568	System And Software For Matched Aligned And Unaligned Storage Instructions
10/757,515	Method And Software For Multithreaded Processor With Partitioned Operations
10/757,516	Programmable Processor And System For Store Multiplex Operation
10/757,524	Programmable Processor And For Partitioned Group Element Selection Operation
10/757,836	Programmable Processor And System For Partitioned Floating-Point Multiply-Add Operation.

Application Number	Title
10/757,851	Method And Software For Partitioned Floating-Point Multiply-Add Operations
10/757,866	Method And Software For Store Multiplex Operation
10/757,925	Method And Software For Partitioned Group Element Selection Operation
10/757,939	Multithreaded Programmable Processor And System With Partitioned Operations

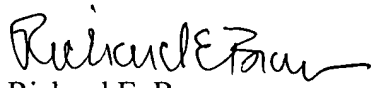
The attached form PTO-1449 includes (but is not exclusively limited to) documents that were cited in on-going litigation proceedings between the assignee of the present application, Dell Inc. and Intel Corp. (U.S. District Court for the Eastern District of Texas, Marshall Division (Civil Action No. 2:04-CV-120(TJW)). This litigation involves seven patents that are in the same family as each of the above applications.

Additionally, some documents were cited in related foreign applications. A copy of the foreign search report or office action is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Richard E. Brown
Registration No. 47,453
Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 REB:llg
Facsimile: 202.756.8087
Date: June 10, 2005

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-129	"IEEE Draft Standard for High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", 1995, pp.1-104, IEEE.	
	L-130	Gerry Kane and Joe Heinrich, "MIPS RISC Architecture" 1992, Publisher: Prentice-Hall Inc., A Simon & Shuster Company, Upper Saddle River New Jersey.	
	L-131	CATHY MAY et al."The Power PC Architecture: A Specification For A New Family of Risc Processors" Second Edition May 1994, pp. 1—518, Morgan Kaufmann Publishers, Inc. San Francisco CA, IBM International Business Machines, Inc.	
	L-132	"IEEE Standard for Scalable Coherent Interface (SCI)" , Published by the Institute of Electrical and Electronics Engineers, Inc. August 2, 2003, pp. 1-248.	
	L-133	DON TOLMIE and Don Flanagan, "HIPPI: It's Not Just for Supercomputers Anymore" Data Communications published May 8, 1995.	
	L-134	Kevin D. Kissell "The Dead Supercomputer Society The Passing Of A Golden Age", February, 1998 pp. 1-2, [http:/www.paralogos.com/DeadSuper].	
	L-136	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X May 1995.	
	L-137	JOE HEINRICH, "MIPS R4000 Microprocessor User's Manual Second Edition"1994 MIPS Technologies, Inc. pp. 1-754.	
	L-138	Litigation proceedings in the matter of *Microunity Systems Engineering, Inc.* v. *Dell, Inc. et al.*, Corrected Preliminary Invalidity Contentions and Exhibits, filed January 12, 2005, Civil Action No. 2:04-CV-120(TJW), U.S. District Court for the Eastern District of Texas Marshall Division.	
	L-139	Ang, StarT Next Generation: Integrating Global Caches and Dataflow Architecture, Proceedings of the ISCA 1992.	
	L-140	Saturn Architecture Specification, published April 29, 1993.	
	L-141	C4/XA Architecture Overview, Convex Technical Marketing presentation dated November 11, 1993 and February 4, 1994.	
	L-142	Convex 3400 Supercomputer System Overview, published July 24, 1991.	
	L-143	Giloi, Parallel Programming Models and Their Interdependence with Parallel Architectures, IEEE Proceedings published September 1993.	
	L-144	PCT International Search Report and Written Opinion dated March 11, 2005, corresponding to PCT/US04/22126	
	L-145	Supplementary European Search Report dated March 18, 2005, corresponding to Application No. 96928129.4	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
043876-0145	**10/646,787**
APPLICANT: **HANSEN, C., et al.**	
FILING DATE: **August 25, 2003**	GROUP: **2183**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	4,658,349 A	05/14/1987	Gafken	
		US	4,852,098	07/25/1989	Brechard et al.	
		US	4,875,161	10/17/1989	Lahti	
		US	4,949,294	08/14/1990	Wambergue	
		US	4,953,073	08/28/1990	Moussouris et al.	
		US	4,959,779	09/25/1990	Weber et al.	
		US	5,113,506	05/12/1992	Moussouris et al.	
		US	5,161,247	11/3/1992	Murakami et al.	
		US	5,208,914	05/04/1993	Wilson et al.	
		US	5,231,646	07/27/1993	Health et al	
		US	5,233,690	08/03/1993	Shelock et al.	
		US	5,268,995	12/07/1993	Diefendorff et al.	
		US	5,347,643 A	09/13/1994	Kondo Nobukazu et al.	
		US	5,412,728 a	05/03/1995	Besnard Christian et al.	
		US	5,430,660 A	07/04/1995	John Hengeveld et al.	
		US	5,471,628	11/28/1995	Phillips et al.	
		US	5,515,520	05/07/1996	Hatta et al.	
		US	5,533,185	07/02/1996	Lentz et al.	
		US	5,590,365	12/31/1996	Ide et al.	
		US	5,636,351	06/03/1997	Lee	
		US	5,742,840	04/21/1998	Hansen et al.	
		US	5,778,412 A	07/07/1998	Gafken	
		US	5,828,869	10/27/1998	Johnson et al.	
		US	5,996,057	11/30/1999	Scales, III et al.	
		US	6,453,368 B2	09/17/2002	Yamamoto	
		US	6,657,908 B1	05/20/2003	Furuhashi	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes3 -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
		JP 3268024	11/28/1991	Hitachi Ltd.			
		EP 0 468 820 A2	01/29/1992	Fujitsu Limited			
		WO 93/01565	01/21/1993	Seiko Epson Corporation			
		CA 1 323 451	10/19/1993	Northern Telecom Ltd.			
		JP 6095843	04/08/1994	IBM			
		EP 0 651 321 A	05/03/1995	Advanced Micro Devices Inc.			
		EP 0 654 733 A1	05/24/1995	Hewlett-Packard			
		JP-S60-217435	10/31/1985	Toshiba Corp.			
		WO 97/07450	02/27/1997	Microunity Systems Engineering, Inc.			

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-1	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," p. 12-21, 28 March 1993, IEEE J. OF SOLID-STATE CIRCUITS.	
	L-2	K. Uchiyama et al., The Gmicro/5OO Superscalar Microprocessor with. Branch Buffers, IEEE Micro, October 1993, p. 12-21.	
	L-3	Ruby B. Lee, Realtime MPEG Video Via Software Decompression on a PA-RISC Processor, IEEE (1995).	
	L-4	Karl M. Guttag et al. "The TMS34010: An Embedded Microprocessor", IEEE June 1988, p. 186-190.	
	L-5	M. Awaga et al., "The μVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation", IEEE Micro, Vol. 13, No. 5, October 1993, p.24-36.	
	L-6	Tom Asprey et al., "Performance Features of the PA7100 Microprocessor", IEEE Micro (June 1993), p. 22-35.	
	L-7	Gove, Robert J., "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conf., March (1994), pp. 215-224.	
	L-8	Woobin Lee, et al., "Mediastation 5000: Integrating Video and Audio," IEEE Multimedia,1994, pp. 50-61.	
	L-9	Karl, Guttag et. al "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, November, 1992, p. 53-64.	
	L-10	TMS32OC8O (MVP) Master Processor User's Guide, Texas Instruments, March, 1995, p. 1-33.	
	L-11	TMS320C80 (MVP) Parallel Processor User's Guide ["PP"]; Texas Instruments March 1995, p. 1-80.	
	L-12	Shipnes, Julie, "Graphics Processing with the 88110 RISC Microprocessor," IEEE COMPCOM, (Spring,1992) pp. 169-174.	
	L-13	ILLIAC IV: Systems Characteristics and Programming Manual, May 1, 1972, p. 1-78.	
	L-14	N. Abel et al., ILLIAC IV Doc. No. 233, "Language Specifications for a Fortran-Like Higher Level Language for ILLIAV IV, August 28, 1970, p. 1-51.	
	L-15	ILLIAC IV Quarterly Progress Report: October, November, December 1969; Published January 15, 1970, pp. 1-15.	
	L-16	N.E. Abel et al., Extensions to Fortran for Array Processing (1970) pp. 1-16.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-17	Morris A, Knapp et al.ILLIAC IV Systems Characteristics and Programming Manual (1972) "Bulk Storage Applications in the ILLIAC IV System," p. 1-10.	
	L-18	Rohrbacher, Donald, et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp 54-59 (August, 1977) (reprinted version pp 119-124).	
	L-19	Siegel, Howard Jay, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6, (June, 1979) (reprinted version pp 110-118).	
	L-20	Mike Chastain, et. al., "The Convex C240 Architecture", Conference of Supercomputing, IEEE 1988, p. 321-329.	
	L-21	Gwennap, Linley, "New PA-RISC Processor Decodes MPEG Video: HP's PA-71 00LC Uses New Instructions to Eliminate Decoder Chip," Microprocessor Report, (January 24, 1994) pp. 16-17.	
	L-22	Patrick Knebel et al., "HP's PA7100LC: A Low-Cost Superscalar PARISC Processor," IEEE (1993), pp. 441-447.	
	L-23	Kurpanek *et* al., "PA7200: A PA-RISC Processor with Integrated High Performance MP Bus Interface," EEEE (1994), pp. 375-82.	
	L-24	Hewlett Packard, PA-RISC 1.1 Architecture and Instruction Set Reference Manual, 3rd ed. Feb. 1994, pp. 1-424.	
	L-25	Margaret Simmons, et. al "A Performance Comparison of Three Supercomputers – Fujitsu VP-2600, NEC SX-3, and Cray Y-MP",. 1991 ACM, p. 150-157.	
	L-26	Smith, J. E., "Dynamic Instruction Scheduling and the Astronautics ZS-1," Computer, Vol. 22, No. 7, July 1989, at 21-35 and/or the Astronautics ZS- 1 computers made used, and/or sold in the United States, pp. 159-173.	
	L-27	Nikhil et al., "T: A Multithreaded Massively Parallel Architecture" Computation Structures Group Memo 325-2 (March 5, 1992) , pp. 1-13.	
	L-28	Undy, et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE pp. 10-22 (1994).	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-29	Feng, Tse-Yun, "Data Manipulating Functions in Parallel Processors and Their Implementations," IEEE Transactions on Computers, Vol. C-23, No. 3, March, 1974 (reprinted version pp. 89-98.	
	L-30	Lawrie, Duncan H., "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. c-24, No. 12, December, 1975 pp. 99-109.	
	L-31	Broomell, George, et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, June, 1983 pp 95-133.	
	L-32	Jain, Vijay, K., "Square-Root, Reciprocal, SINE/COSINE, ARCTANGENT Cell for Signal and Image Processing," IEEEICASSP'94 April, 1994 , pp II-521 -- II-524.	
	L-33	Spaderna et al., "An Integrated Floating Point Vector Processor for DSP and Scientific Computing", 1989 IEEE, ICCD, October 1989 p. 8-13.	
	L-34	Gwennap, Linley, "Digital, MIPS Add Multimedia Extensions," Microdesign Resources Nov. 18, 1996 pp. 24-28.	
	L-35	Toyokura, M., "A Video DSP with a Macroblock-Level-Pipeline and a SIMD Type Vector-Pipeline Architecture for MPEG2 CODEC," ISSCC94, Section 4, Video and Communications Signal Processors, Paper WP 4.5, 1994 pp. 74-75.	
	L-36	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," Nobuhiro Ide, et. Al. IEEE Tokyo Section, Denshe Tokyo No. 32, 1993, p. 103-109.	
	L-37	Papadopoulos et al., "*T: Integrated Building Blocks for Parallel Computing," ACM (1993) p. 824- and p. 625-63.5	
	L-38	Ruby B. Lee, "Accelerating Multimedia with Enhanced Microprocessors," IEEE Micro April 1995 p. 22-32.	
	L-39	Ruby B. Lee, "Realtime MPEG Video Via Software Decompression on a PA-RISC Processor," IEEE (1995), pp. 186-190.	
	L-40	K. Diefendorff , M. Allen, The Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, p. 157-162.	
	L-41	Kristen Davidson, Declaration of Kristen Davidson, p. 1 and H. Takahashi et al., A 289 MFLOPS Single Chip Vector Processing Unit, The Institute of Electronics, Information, and Communication Engineers Technical Research Report, 5/28/92, pp. 17-22.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-42	Kristen Davidson, Declaration of Kristen Davidson, p. 1 and M. Kimura et al., Development of Ginicro 32-bit Family of Microprocessors, Fujitsu Semiconductor Special Part 2, Vol. 43, No. 2, February 1992.	
	L-43	Bit Manipulator," IBM Technical Disclosure Bulletin, November, 1974, pp 1576-1576 https://www.delphion.com/tdbs/tdb?order=75C+0016.	
	L-44	"Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, July, 1986, p. 699-701 https://www.delphion.com/tdbs/tdb?order=86A+61578.	
	L-45	Motorola MC88110 Second Generation RISC Microprocessor User's Manual (1991).	
	L-46	Berkerele, Michael J., "Overview of the START (*T) Multithreaded Computer" IEEE January 1993, p. 148-1 56.	
	L-47	Diefendorff, et al., "Organization of the Motorola 88110 Superscalar RISC Microprocessor" IEEE Micro April, 1992, p.39-63;	
	L-48	Barnes, et al., The ILLIAC IV Computer, IEEE Transactions on Computers, vol. C-17, no. 8, August 1968.	
	L-49	Ruby B. Lee et al., Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7 100LC Processors, Hewlett-Packard J. April 1995, p.60-68.	
	L-50	Ruby B. Lee, "Realtime MPEG Video Via Software Decompression on a PA-RISC Processor," IEEE 1995, p.186-192.	
	L-51	"The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," Robert J. Gove, IEEE DSP Workshop (1994).	
	L-52	Convex Assembly Language Reference Manual, First Ed., December 1991.	
	L-53	Convex Architecture Reference Manual (C Series), Sixth Edition, Convex Computer Corporation (April 1992).	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-54	Manferdelli, et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," submitted to SPIE Annual International Technical Symposium, Sm Diego, Society of Photo Optical Instrumentation Engineers, July 30, 1980, p. 1-8.	
	L-55	Paul Michael Farmwald, Ph.D. "On the Design of High-Performance Digital Arithmetic Units," Thesis, August 1981, p. 1-95.	
	L-56	GsAs Supercomputer Vendors Hit Hard,, Electronic News,1/31/94, 1991, pp. 32.	
	L-57	Convex Adds GaAs System, Electronic News, June 20, 1994.	
	L-58	Kevin Wadleigh et al., High-Performance FFT Algorithms for the Convex C4/XA Supercomputer, Journal of Super Computing, Vol. 9, pp. 163-78 (1995).	
	L-59	Peter Michielse, "Programming the Convex Exemplar Series SPP System, Parallel Scientific Computing, First Intl Workshop, PARA '94, June 20-23, 1994, pp. 375-82.	
	L-60	Ryne, Robert D., "Advanced Computers and Simulation," Los Alamos National Laboratory IEEE 1 993, p. 3229-3233.	
	L-61	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) p. 124-132.	
	L-62	Bell, Gordon, "Ultracomputers: A Teraflop Before its Time," Comm.'s of the ACM Aug. 1992 pp. 27-47.	
	L-63	Geist, G. A., "Cluster Computing: The Wave of the Future?" Oak Ridge National Laboratory, 84OR2 1400 May 30, 1994, p. 236-246.	
	L-64	Vetter et al., "Network Supercomputing," IEEE Network May 1992, p. 38-44.	
	L-65	Renwick, John K." Building a Practical HIPPI LAN," IEEE 1992, p. 355-360.	
	L-66	Tenbrink, et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science 1994 p. 1-4.	
	L-67	Arnould *et* al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM 1989 p. 1-12.	
	L-68	Watkins, John, et al., "A Memory Controller with an Integrated Graphics Processor," IEEE 1993 p 324-336.	
	L-69	"Control Data *6400/6500/ 6600* Computer Systems, Instant SMM Maintenance Manual.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-70	"Control Data *6400/6500/ 6600* Computer Systems, SCOPE Reference Manual, September1966.	
	L-71	"Control Data *6400/6500/ 6600* Computer Systems, COMPASS Reference Manual, 1969.	
	L-72	Tolmie, Don, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM?" Los Alamos National Laboratory Rep. No. LA-UR 94-3994 (1994).	
	L-73	ILLIAC IV: Systems Characteristics and Programming Manual, May 1, 1972.	
	L-74	1979 Annual Report: The S-1 Project Vol. 1 Architecture 1979.	
	L-75	1979 Annual Report: The S-1 Project Vol.2 Hardware 1979.	
	L-76	S-1 Uniprocessor Architecture, April 21, 1983 (UCID 19782) ***See*** also S-1 Uniprocessor Architecture (SMA-4), Steven Cornell;	
	L-77	Broughton, et al., The S-1 Project: Top-End Computer Systems for National Security Applications, October 24, 1985.	
	L-78	Convex Data Sheet C4/XA High Performance Programming Environment, Convex Computer Corporation.	
	L-79	Bowers et al., "Development of a Low-Cost, High Performance, Multiuser Business Server System," Hewlett-Packard J. Apr. 1995 p. 79-84.	
	L-80	Mick Bass et al., "The PA 7100LC Microprocessor: A Case Study of Design Decisions in a Competitive Environment Hewlett-Packard J. April 1995, p. 12-18.	
	L-81	Mick Bass, et. al. "Design Methodologies for the PA 7100LC Microprocessor", Hewlett Packard Journal April 1995 p. 23-35.	
	L-82	Wang, Chin-Liang, "Bit-Level Systolic Array for Fast Exponentiation in GF (2Am)," IEEE Transactions on Computers, Vol. 43, No. 7, July, 1994 p. 838-841.	
	L-83	Markstein, P.W., "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, Jan. 1990 p. 111-119.	
	L-84	Donovan, Walt, et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, January, 1995 p. 51- 61.	
	L-85	Ware et al., 64 Bit Monolithic Floating Point Processors, IEEE Journal Of Solid-state Circuits, Vol. Sc-17, No. 5, October 1982, pp. 898-907.	
	L-86	Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability" (1 993) at 475, p. 898-907.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-87	Hwang & Degroot, "Parallel Processing for Supercomputers & Artificial Intelligence," 1993.	
	L-88	Nienhaus, Harry A., "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, 1989 pp 1103-1105.	
	L-89	Eisig, David, et al., "The Design of a 64-Bit Integer Multiplier/Divider Unit," IEEE 1993 pp 171-178.	
	L-90	Margulis, Neal, "i860 Microprocessor Architecture," Intel Corporation 1990.	
	L-91	Intel Corporation, 3860 XP Microprocessor Data Book" (May 1991).	
	L-92	Hewlett-Packard, "HP 9000 Series 700 Workstations Technical Reference Manual Model 712 (System)" January 1 994.	
	L-93	Ruby Lee, et al., Pathlength Reduction Features in the PA-RISC Architecture Feb. 24-28, 1992 p. 129-135.	
	L-94	Kevin Wadleigh et al., High Performance FFT Algorithms for the Convex C4/XA Supercomputer, Poster, Conference on Supercomputing, Washington, D.C., Nov. 1994.	
	L-95	Fields, Scott, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin- Madison 1993 p. 1-8.	
	L-96	Litzkow *et* al., "Condor - A Hunter of Idle Workstations," IEEE (1 988) p. 104-111.	
	L-97	Gregory Wilson, The History of the Development of Parallel Computing" http://ei.cs.vt.edu/-history/Parallel.html, p. 1-38.	
	I-98	Marsha Jovanovic and Kimberly Claffy, Computational Science: Advances Through Collaboration" "Network Behavior" San Diego Supercomputer Center 1993 Science Report, p.1-11 [http://www.sdsc.edu/Publications/SR93/network_behavior.html].	
	L-99	National Science Foundation (NSF) [www.itrd.gov/pubs/blue94/section.4.2.html] 1994.	
	L-100	Intel Corporation, "Paragon User's Guide" (Oct. 1993).	
	L-101	Turcotte, Louis H., "A Survey of Software Environments for Exploiting Networked Computing Resources" Engineering Research Center for Computational Field Simulation June 11, 1993, p. 1-150.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-102	Patterson, Barbara, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip" Motorola Computer Group, p. 1-3 [http://badabada.org/misc/mvme197_announce.txt].	
	L-103	Culler, David E., et al., "Analysis Of Multithreaded Microprocessors Under Multiprogramming", Report No. UCBICSD 921687, May 1992 p.1-17.	
	L-104	James Laudon et al., "Architectural And Implementation Tradeoffs In The Design Of Multiple-Context Processors", CSL-TR-92-523, May 1992 p. 1-24.	
	L-105	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," 28 IEEE Custom Integrated Circuits Conference, 1992, p. 30.2.1-30.2.4.	
	L-106	High Speed DRAMs, Special Report, IEEE Spectrum, vol. 29, no. 10, October 1992.	
	L-107	Moyer, Steven A., "Access Ordering Algorithms for a Multicopy Memory," IPC-TR-92-0 1 3, December 18, 1992.	
	L-108	Moyer, Steven A., "Access Ordering and Effective Memory Bandwidth," Ph.D. dissertation, University of Virginia, April 5, 1993.	
	L-109	"Hardware Support for Dynamic Access Ordering: Performance of Some Design Options", Sally McKee, Computer Science Report No. CS-93-08, August 9, 1993.	
	L-110	McGee et al., "Design of a Processor Bus Interface ASIC for the Stream Memory Controller" p. 462-465.	
	L-111	McKee et al., "Experimental Implementation of Dynamic Access Ordering ," August 1, 1993, p. 1-10.	
	L-112	McKee et al., Increasing Memory Bandwidth for Vector Computations, Technical Report CS-93-34 August 1, 1993, p.1-18.	
	L-113	Sally A. McKee et al., "Access Order and Memory-Conscious Cache Utilization" Computer Science Report No. CS-94- 10, March 1, 1994, p.1-17.	
	L-114	McKee, et. al., "Bounds on Memory Bandwidth in Streamed Computations," Computer Science Report CS-95-32, March 1, 1995.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-115	McKee, Sally A., "Maximizing Memory Bandwidth for Streamed Computations," A Dissertation Presented to the Faculty of the School of Engineering and Applied Science at the University of Virginia, May 1995.	
	L-116	A Systematic Approach to Optimizing and Verifying Synthesized High-Speed ASICs", Trevor Landon, et. Al. , Computer Science Report No. CS-95-51, December 11, 1995.	
	L-117	"Control Data *6400/6500/ 6600* Computer Systems Reference Manuals" 1969 available at http:/led-thelen.org/comp-hist/CDC-6600-R-M.html ("CDC 6600 Manuals").	
	L-118	"Where now for Media processors?", Nick Flaherty, Electronics Times, August 24, 1998.	
	L-119	George H. Barnes et al., The ILLIAC IV Computer[1] , [1]IEEE Trans., C-17 vol. 8, pp. 746-757, August 1968.	
	L-120	J.E. Thornton, Design of a Computer - The Control Data *6600* (1970) .	
	L-121	Gerry Kane, PA-RISC 2.0 Architecture", Chp. 6 Instruction Set Overview, Prentice Hall isbn 0-13-182734-0, p. 6-1—6-26.	
	L-122	Cosoroaba, A.B., "Synchronous DRAM products revolutionize memory system design," Fujitsu Microelectronics, Southcod95 May 709 1995 .	
	L-123	Intel 450KX/GX PCIset, Inetel Corporation, 1996..	
	L-124	Baland, Granito, Marcotte, Messina, Smith, "The IBM System1360 Model 91 : Storage System" IBM System Journal, January, 1967, pp. 54-68.	
	L-125	File History of U.S. Patent Application No. 08/340,740 (filed November 16, 1994).	
	L-126	File history of U.S. Patent Application No. 07/663,314 (filed March 1, 1991).	
	L-127	S.S. Reddi et. al. "A Conceptual Framework for Computer Architecture" Computing Surveys,. Vol. 8, No. 2, June 1976.	
	L-128	Yulun Wang, et al, "The 3DP: A processor Architecture for Three-Dimensional Applications, January 1992, p. 25-36.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.